UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,552	02/27/2002	Hiroshi Nakamura	001701.00672	8483

22907 7590 03/26/2004

BANNER & WITCOFF
1001 G STREET N W
SUITE 1100
WASHINGTON, DC 20001

EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,552	NAKAMURA, HIROSHI	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/656831.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 12/23/2003. Applicant's arguments are persuasive. A new ground of rejection is introduced.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 28-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bill et al. (USP 5059815) (previous cited) in view of Change et al (USP 5734290) (newly cited) and Applicant's admitted prior art figure 1.

As to claims 28, 42, and 56, Bill et al. discloses in figure 3 a voltage generating/transferring circuit comprising: a boost unit group including a plurality of boost units (350, 360) series-connected between input node (C) and node (VOUT) directly, each boost unit having input and output portions; a first transistor (310) connected between the input node and a node for receiving a first voltage (Vpp), a second transistor (350, 360) included in each boost unit; a second capacitor (C3, C4) included in each boost unit and connected to the input portion thereof; and a third transistor (340) connected to the gate of the first transistor, wherein both a gate and a drain of the second transistor are connected to the input portion, a source of the second transistor is connected to the output portion, and a gate of the first transistor is directly connected to the input portion of one of boost unit (360), a charge moves between the output portion of the boost units and the input portion of another of the boost units. Thus, figure 3

shows all limitations of the claims except for a first capacitor having one end which is connected to an output node, and another end which is receives a first oscillation signal. However, Change et al.'s figure 1 shows a charge pump circuit having a capacitor (C1) having one end connected to output node Vout and the other end connected to oscillation signal (ϕ1) for the purpose of generating output voltage Vout higher than the input of the last stage, thereby increasing the output voltage. Therefore, it would have been obvious to one having ordinary skill in the art to add a capacitor (similar to Bill et al.'s capacitor) coupled between Bill et al.'s output node Vout and the first oscillation signal for the purpose of further boosting the output voltage in order to generating an output voltage which is higher than the input of the last stage, thereby increasing the output voltage. The combination of prior Bill et al. and Change et al. references fails to shows "when the third transistor turns on and transfers a second voltage from a source of the third transistor to a drain of the third transistor without voltage drop, the first transistor turns off and the voltage generating/transferring circuit becomes disabled. However, Applicant's prior art figure 1 shows a voltage generating/transferring circuit having a third transistor QN5 connected to the gate of the first transistor QN1 for enable and disable the voltage generating/transferring circuit. Therefore, it would have been obvious to one having ordinary skill in the art to employ the prior art figure 1's teaching for each of Bill et al.'s transistors 320, 330, 340 for the purpose of further providing enable and disable function to the circuit (by providing Vcc to the gate of transistors 320, 330 and 340 and providing input signal to the drain of transistors 320, 330 and 340).

As to claims 29, 36, 43, 50, 58, and 65, figure 2 shows a fourth transistor (250) which has a gate connected to the output node, and transfers a third voltage (VppI), wherein a fourth

voltage at the gate of the fourth transistor is equal to or greater than a sum of the third voltage and a threshold voltage of the fourth transistor (V270 = VppI + Vgate-source, wherein Vgate-source = threshold voltage) in transferring the third votlage.

As to claims 30, 44 and 59, Bill et al.'s figure 3 shows a second oscillation signal /Φ is input to an even-numbered boost unit from the input node, a third oscillation signal ϕ is input to an odd-numbered boost unit from the input node, and the second and third oscillation signals have opposite phases or different timings.

As to claims 31, 45 and 60, it is inherent for gate and source voltage levels of the first transistor gradually rise while changing in opposite phases.

As to claim 32, 46 and 61, it is inherent that the second voltage is 0V.

As to claims 33-35, 41, 47-49, 55, 62-64 and 70, figures 1a and 3 show all limitations of the claims except for a threshold voltage of the second transistor (or the second transistor in at least one of the boost units) is lower than a threshold voltage of the first transistor; or a transistor having a threshold voltage lower than the threshold voltage of the first transistor is arranged in a boost unit closest to the output node; a threshold voltage of a transistor in a boost unit on the output node side is lower than a threshold voltage of a transistor in a boost unit on the input node side. However, it is well known in the art that thresholds of the diode connected transistors e.g. 350, 360... is invert proportional to the level of the voltage output. Therefore, it would have been obvious to one having skill in the art to reduce the threshold of all diode connected transistors in the boost unit for the purpose of increasing the output voltage level.

As to claims 37, 51 and 66, the modified Bill et al.'s figures 2 and 3 show a fourth transistor (250) connected to the output node, and transfers a third voltage, a fifth transistor (the

modified transistor 320) connected to a gate of the fourth transistor, wherein when the fifth transistor turns on (when the input signal at the drain of 320 is low) and transfers a fourth voltage from a source (drain) (the drain and source of MOS transistor are the same. They are named base on the direction of current going through the transistor) of the fifth transistor to a drain (source) of the fifth transistor without voltage drop, the fourth transistor turns off and the voltage generating/transferring circuit becomes disabled.

As to claim 38, 52 and 67, it is inherent that the fourth voltage is 0V.

As to claim 39, 53 and 68, the modified Bill et al.'s figures 2 and 3 show a fourth transistor (the modified transistor 320) connected to a the output node, wherein when the fourth transistor turns on (when the input signal at the drain of 320 is low) and transfers a third voltage from a source (drain) (the drain and source of MOS transistor are the same. They are named base on the direction of current going through the transistor) of the fourth transistor to a drain (source) of the fifth transistor without voltage drop, the voltage generating/transferring circuit becomes disabled.

As to claims 40, 54 and 69, Bill et al.'s figure 3 shows the first oscillation signal and an oscillation signal (Φ) which is input to the boost unit connected to the first capacitor have opposite phased or different timings.

As to claim 57, figure 3 shows a source or drain of the first transistor is directly connected to the input node.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 12, 2004

Terry D. Cunningham
Primary Examiner